REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicant amends claims 1-5, and adds new claims 7-17. Accordingly, claims 1-17 are pending in the application.

Applicant thanks the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority document(s).

The Examiner is respectfully requested to state whether the drawings are acceptable.

Claims 1-4 are amended for non-statutory reasons, to delete reference numerals.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

35 U.S.C. § 102

The Office Action rejects claims 1-6 under 35 U.S.C. § 102 over Nakatani et al. U.S. Patent 6,667,657 ("Nakatani").

Applicant respectfully traverses those rejections for at least the following reasons.

Claim 1

Among other things, the amplifier device of claim 1 includes a bias voltage applied to an amplifier means for adjusting a current determining a noise level of the amplifier means.

Applicant respectfully submits that Nakatani does not disclose any such feature.

The Office Action states that Nakatani discloses such a feature, but does not cite any elements or text in Nakatani that supposedly discloses such features. Applicant respectfully submits that Nakatani discloses an arrangement where a switch 22 is connected in parallel with an amplifying circuit (10/10A), for turning the amplifying circuit (10/10A) ON and OFF without having to switch the supply voltage therefore, Vcc, to ground, this permitting a faster switching speed (see col. 9, lines 8-24). Thus, amplifying circuit (10/10A) **does not operate** when the switch 22 is in an

ON state (see, e.g., col. 8, lines 32-39; Abstract at lines 1-6; col. 2, lines 50-56; etc.). Therefore, there is no bias voltage applied to amplifying circuit (10/10A) for adjusting a current determining a noise level of the amplifier means.

Accordingly, for at least these reasons, claim 1 is deemed patentable over Nakatani.

Claims 2-4

Claims 2-4 depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 2

In the device of claim 2, feedback loop includes at least a first resistor and a second resistor connected in parallel to each other, and wherein the second resistor is connected in series with a switch controlled by the mode selection means.

Applicant respectfully submits that Nakatani does not disclose such an arrangement of features.

The Office Action states that the switch 22 can operate as a resistor "as well as a switch."

However, in the actual circuit of FIG. 1 of Nakatani, MOS 22 is configured to operate as a switch – not as a resistor. This is clear throughout the teaching of Nakatani (e.g., col. 7, lines 24-25; col. 8, lines 17-20, 39-43, 47-51, 55-57; col. 9, lines 1-2, 24-40) and Nakatani does not disclose or suggest that MOS 22 of FIG. 1 should ever be configured to be applied with appropriate gate voltages to operate as a resistor.

Accordingly, for at least these additional reasons, claim 2 is deemed patentable over Nakatani.

Claim 3

The device of claim 3 includes mode selection means arranged to control the feedback loop and the bias voltage to provide a third mode providing high gain and high current.

Applicant respectfully submits that Nakatani does not disclose such an

arrangement of features.

The Office Action states that "[t]he circuit of Nakatani is the same as the circuit claimed" and therefore (supposedly) "capable to handle a 'third mode' for medium signals without modification.

Applicant respectfully submits that this statement is false, and does not address what is actually recited in claim 3.

The circuit of Nakatani is very clearly **NOT** the same as the circuit claimed. There are many elements in both FIG. 1 and FIG. 2 (capacitor 21, capacitor 105, switch 106, switch 108, etc.) that are not recited anywhere in claim 3. So it is not possible that "[t]he circuit of Nakatani is ***the same as*** the circuit claimed."

Furthermore, claim 3 recites **mode selection means** arranged to provide a third mode. No such mode selection means are disclosed by Nakatani or identified anywhere in the Office Action. Nor does the Office Action explain how any such third mode is possible with the circuit of FIGS. 1 and 2 of Nakatani. Applicant respectfully submits that it is NOT possible, because Nakatani teaches that when switch 22 is in the ON state, then amplifying circuit (10/10A) does not even operate!

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 3 is patentable over Nakatani.

Claim 5

Among other things, in the method of claim 5, the amplifier means is turned on in both the first mode and second mode to provide a higher gain and lower noise figure in the first mode, and a lower gain and higher noise figure in the second mode.

As explained above with respect to claim 1, amplifying circuit (10/10A) does not operate when the switch 22 is in an ON state. Being inoperative in the state where switch 22 is ON, amplifying circuit (10/10A) does not provide either a gain or noise figure for the amplifying device.

Accordingly, for at least these reasons, claim 5 is deemed patentable over Nakatani.

Claim 6

Claim 6 depends from claim 5 and is deemed patentable for at least the

reasons set forth above with respect to claim 5, and for the following additional reasons.

The method of claim 6 includes amplifying the signal in a third mode providing high gain and high current for medium signals.

As explained above with respect to claim 3, Applicant respectfully submits that Nakatani does not disclose any method including a third mode, and in particular, the third mode recited in claim 6.

Also, *arguendo*, even **IF** it was true that Nakatani was "capable to handle a 'third mode'" as alleged in the Office Action, Nakatani could not possibly anticipate the **method** of claim 6 that includes actual operation in that third mode, unless such an actual operation was expressly or inherently disclosed by Nakatani. Here, Nakatani does not expressly or inherently disclose operating in any such third mode, nor does the Office Action even allege that it does.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 6 is patentable over Nakatani.

NEW CLAIMS 7-17

Applicant respectfully submits that new claims 7-17 are all patentable over the cited prior art for at least the following reasons.

Claims 7-9

Claims 7-9 depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1, and for the following additional reasons. In the device of claim 7, the amplifier means is an operational amplifier; in the device of claim 8, the high gain and the low-gain are both greater than unity; and in claim 9 the high gain and the low-gain are both greater than 10 dB.

None of these features are disclosed in Nakatani. Indeed, these features are not possible in Nakatani which teaches that the amplifying circuit (10/10A) is inoperative in the case of a high input signal and therefore has no gain!

Accordingly, for at least these additional reasons, Applicant respectfully submits that claims 7-9 are patentable over Nakatani.

Claim 10-11

Claim 10-11 depend from claim 5 and are deemed patentable for at least the reasons set forth above with respect to claim 5, and for the following additional reasons. In the method of claim 10, the high gain and the low-gain are both greater than unity. Meanwhile, the method of claim 6, the high gain and the low-gain are both greater than 10 dB.

None of these features are disclosed in Nakatani. Indeed, these features are not possible in Nakatani which teaches that the amplifying circuit (10/10A) is inoperative in the case of a high input signal and therefore has no gain!

Accordingly, for at least these additional reasons, Applicant respectfully submits that claims 10-11 are patentable over Nakatani.

Claim 12

Among other things, the device of claim 12 includes an amplifier having a first input adapted to receive a radio frequency signal, a second input, and an output adapted to output an amplified RF signal; a bias voltage circuit connected to the second input of the amplifier, the bias voltage circuit being adapted to supply a bias voltage to the second input of the amplifier that is at least selectable between a first bias voltage value and a second bias voltage value.

Applicant respectfully submits that Nakatani does not disclose a device including this combination of features.

Also among other things, the device of claim 12 includes

Claims 13-17

Claim 13-17 depend from claim 12 and are deemed patentable for at least the reasons set forth above with respect to claim 12, and for the following additional reasons.

Each of the claims 13-17 specifically recites features that are not disclosed or suggested by Nakatani (e.g., the mode selection means is further adapted to provide a third mode providing high gain and high current; the amplifier is an operational amplifier; the feedback path includes at least a first resistor and a second resistor

connected in parallel to each other, wherein the second resistor is connected in series with a switch controlled by the mode selection means; the bias voltage circuit includes: a third resistor connected between a bias supply voltage and the second input of the amplifier; a fourth resistor connected to ground; and a second switch connected between the second input of the amplifier and the second resistor).

Accordingly, for at least these additional reasons, Applicant respectfully submits that claims 13-17 are patentable over Nakatani.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-17 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Date: 24 April 2006

By: _____
Kenneth D. Springer
Registration No. 39,843

VOLENTINE FRANCOS & WHITT, P.L.L.C.
One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283.0724
Facsimile No.: (571) 283.0740